REMARKS/ARGUMENTS

This case has been carefully reviewed and analyzed in view of the Official

Action dated 12 January 2005. Responsive to the rejections made in the Official

Action, Claims 1 – 4 have been amended to correct the language thereof and/or the

combination of elements which form the invention of the subject Patent

Application.

In the Official Action, the Examiner objected to the Specification due to

several informalities therein. Accordingly, the Specification has been amended to

correct those informalities kindly noted by the Examiner, as well as several others

that were found therein.

In the Official Action the Examiner rejected Claims 1 – 3 under 35 U.S.C.

§ 103, as being anticipated by Ichikawa et al., U.S. Patent No. 5,684,830. Claim 4

was rejected under 35 U.S.C. § 103, as being unpatentable over Ichikawa et al.

Before discussing the prior art relied upon by the Examiner, it is believed

beneficial to first briefly review the structure of the invention of the subject Patent

Application, as now claimed. The invention of the subject Patent Application is

directed to an integrated circuit receiver available for infrared or ultrasonic

transmission with digital filtering. The receiver includes an infrared receiver or

ultrasonic transducer for receiving a transmitted signal from outside of the

integrated circuit receiver and producing a modulated carrier signal at an output

thereof. The receiver includes an amplifier having an input connected to the

output of the infrared receiver or ultrasonic transducer for amplifying the

modulated carrier signal to provide an amplified signal at an output of the

amplifier. The integrated circuit receiver further includes a digital filter having an

input connected to the output of the amplifier for filtering out a carrier component

from the amplified signal to recover an original digital data signal. The digital

filter has a sampling frequency with a period greater than a period of a frequency

of the carrier component. The aforesaid combination provides a very simple and

"low parts count" circuit for digitally filtering and demodulating the infrared or

ultrasonically transmitted signal.

In contradistinction, the Ickikawa et al. reference discloses a noise

removing device and data communication apparatus utilizing a transmitting signal

modulated by a data signal to be transmitted. Referring to the prior art receiver

shown in Figs. 29 through 31, such uses a digital filter having an edge detecting

section 352 which provides an output to the demodulating section 355 responsive

to timing signals provided by a counter 353. The counter 353 receives an external

clock signal from a UART clock to set up the edge detecting section 352 and reset

the demodulating section 355. The counter 353 sets up the edge detecting section

352 by means of an edge detection activating section 354, after a time

corresponding to ½ bit from the time of receiving a pulse of the analog input

(modulated carrier) signal, column 4, lines 2 – 8. Thus, as the edge detecting

section 352 is reset at the rate of ½ bit time, the counter must provide the clock

frequency of at least twice the carrier frequency and thus does not provide for <u>a</u>

<u>digital filter having a sampling frequency with a period greater than a period of a</u>

<u>frequency of the carrier component,</u> as now claimed. Still further, the counter

section 353 returns the level of the output of the demodulating section 355 to high

after "one bit time" from the time of receiving the pulse, column 4, lines 8 – 10.

Thus, the demodulating section is reset by a clock signal from the counter that is at

least equal to the carrier frequency. Here again, such then fails to provide for a

sampling frequency with a period that is greater than the period of the frequency

of the carrier component. Still further, as the reset time of the demodulating

section is twice that of the edge detecting section, the reference fails to disclose

<u>the fixed-interval sample circuit having a sampling period **equal** to the reset period</u>

<u>of the fixed interval reset circuit,</u> as now claimed in Claim 2.

In the embodiment shown in Fig. 5 of the reference, the received modulated

signal has a carrier frequency of 500 kHz which is input to the edge detecting

section 42, column 13, lines 3 – 11. The edge detecting section provides an output

to the sampling section 44 in synchronization with a sampling clock signal having

a frequency of 1.8 MHz, column 13, lines 11 – 21. Thus, as the sampling

frequency for the digital filter is significantly greater than the carrier frequency, it

likewise has a sampling period which is much smaller than the period of the

carrier frequency. So, here again, the reference fails to disclose <u>the digital filter</u>

<u>having a sampling frequency with a period greater than a period of a frequency of</u>

the carrier component. Accordingly, the reference also fails to disclose <u>the fixed-integral reset circuit having a reset period greater than the period of the frequency of the carrier component</u>, as defined in Claim 2. Quite the contrary, the reference teaches the reset and sampling periods being substantially smaller than the period of the carrier component.

As the reference fails to disclose each and every one of the elements of the invention of the subject Patent Application, it cannot anticipate that invention. Further, as the reference fails to suggest such a combination of elements, and in fact teaches away from the combination of the invention of the subject Patent Application, it cannot make obvious that invention either. While it is believed that Claims 3 and 4 provide further patentably distinct limitations, those claims are at least patentably distinct for the same reasons as Claim 1.

For all the foregoing reasons, it is now believed that the subject Patent Application has been placed in condition for allowance, and such action is respectfully requested.

Respectfully submitted,
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